

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# MOS FIELD EFFECT TRANSISTOR NP55N04SUG

## SWITCHING N-CHANNEL POWER MOSFET

### DESCRIPTION

The NP55N04SUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

### FEATURES

- Channel temperature 175 degree rating
- Super low on-state resistance  
 $R_{DS(on)} = 6.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 28 \text{ A)}$
- Low input capacitance  
 $C_{iss} = 3400 \text{ pF TYP. (} V_{DS} = 25 \text{ V)}$

### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

	Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	40	V
	Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
	Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	±55	A
	Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±220	A
<R>	Total Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>T1</sub>	77	W
	Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.2	W
	Channel Temperature	T <sub>ch</sub>	175	°C
	Storage Temperature	T <sub>stg</sub>	-55 to +175	°C
	Repetitive Avalanche Current <sup>Note2</sup>	I <sub>AR</sub>	30	A
	Repetitive Avalanche Energy <sup>Note2</sup>	E <sub>AR</sub>	90	mJ

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

**2.** T<sub>ch</sub> ≤ 150°C, V<sub>DD</sub> = 20 V, R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = 20 → 0 V

### THERMAL RESISTANCE

<R>	Channel to Case Thermal Resistance	R <sub>th(ch-C)</sub>	1.95	°C/W
	Channel to Ambient Thermal Resistance	R <sub>th(ch-A)</sub>	125	°C/W

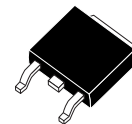
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### ORDERING INFORMATION

PART NUMBER	PACKAGE
NP55N04SUG	TO-252 (MP-3ZK)

(TO-252)

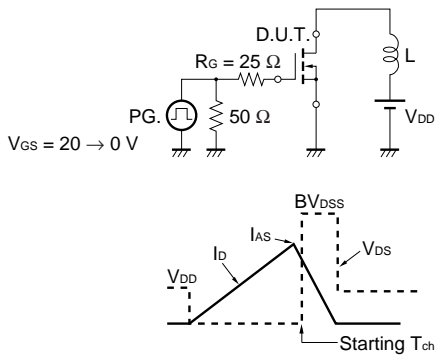


**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**

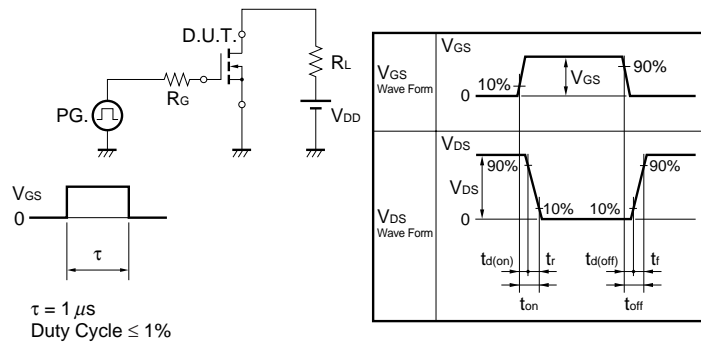
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			1	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 28 A	12	23		S
Drain to Source On-state Resistance <sup>Note</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 28 A		5.0	6.5	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V,		3400	5100	pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V,		320	480	pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		210	380	pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 28 A,		30	66	ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V,		52	130	ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		78	156	ns
Fall Time	t <sub>f</sub>			12	30	ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 32 V,		63	95	nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V,		12		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 55 A		20		nC
Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-D)</sub>	I <sub>F</sub> = 55 A, V <sub>GS</sub> = 0 V		0.94	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 55 A, V <sub>GS</sub> = 0 V,		37		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		40		nC

**Note** Pulsed

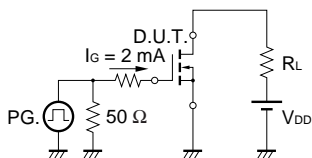
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



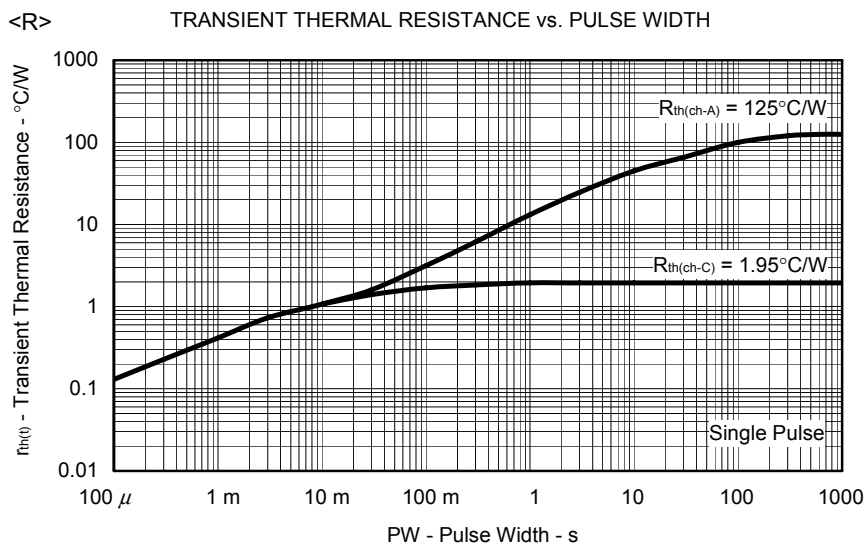
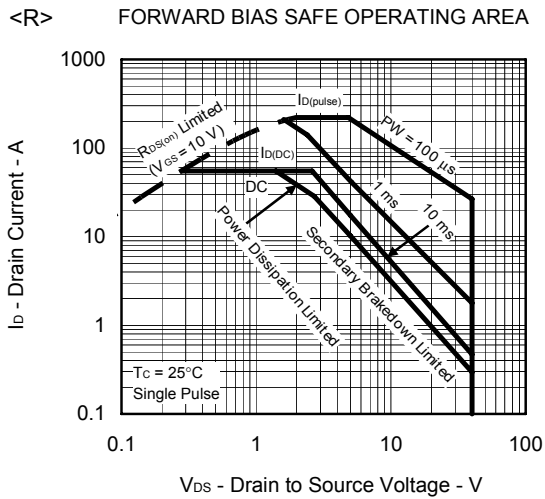
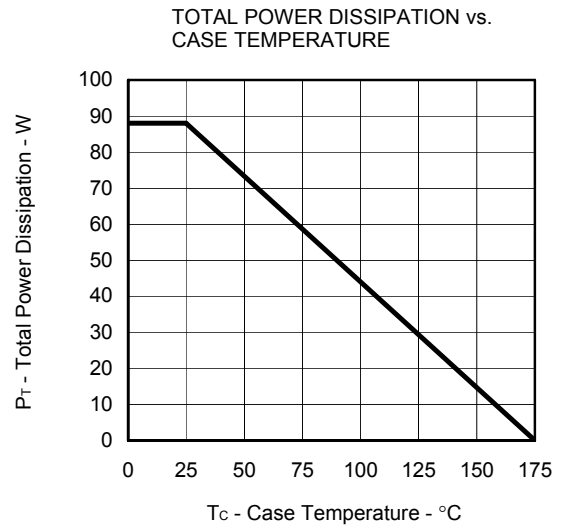
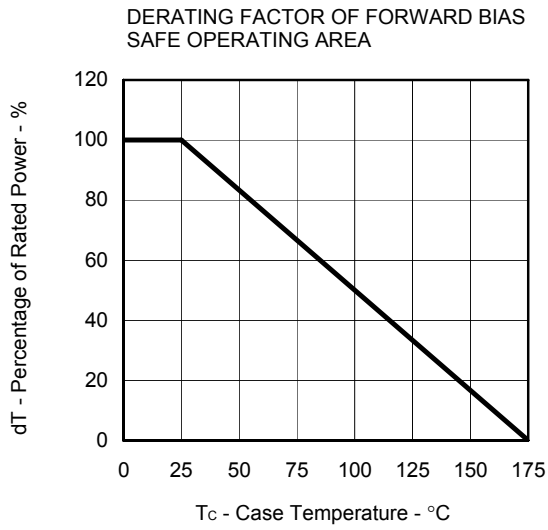
**TEST CIRCUIT 2 SWITCHING TIME**



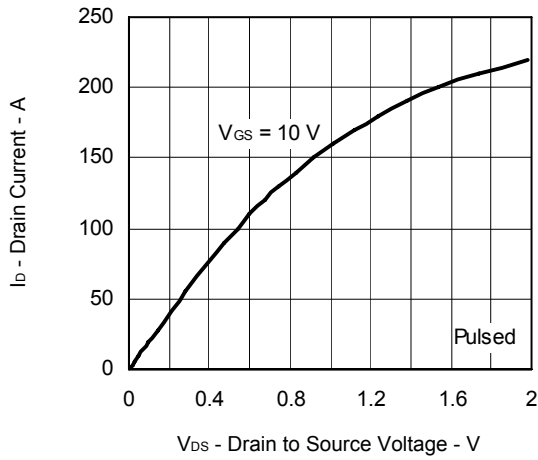
**TEST CIRCUIT 3 GATE CHARGE**



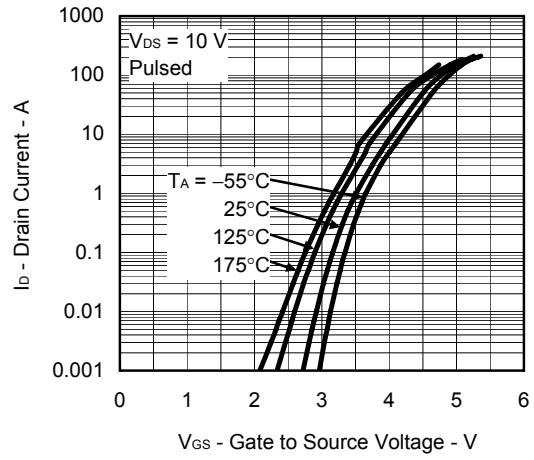
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)



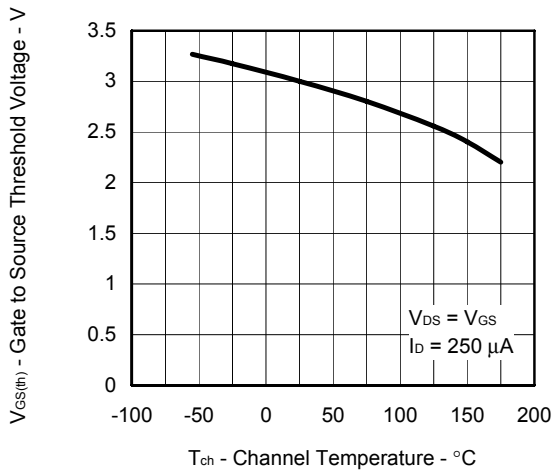
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



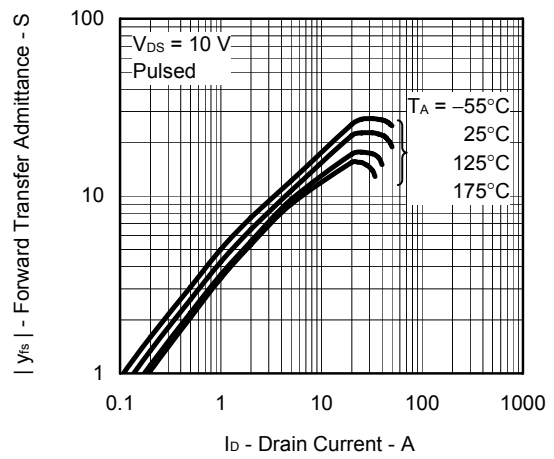
FORWARD TRANSFER CHARACTERISTICS



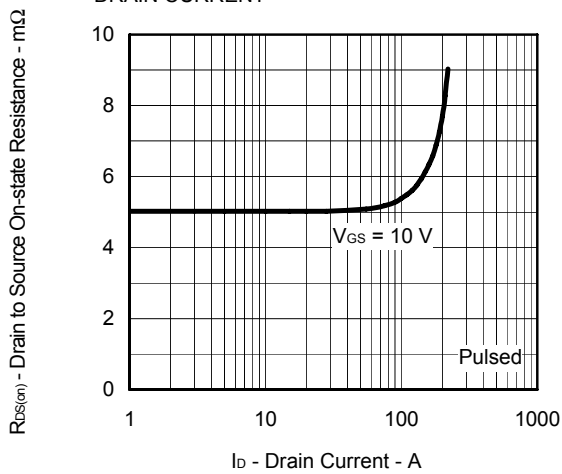
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



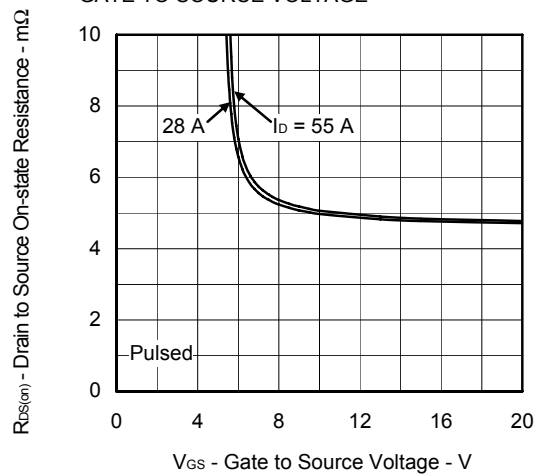
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



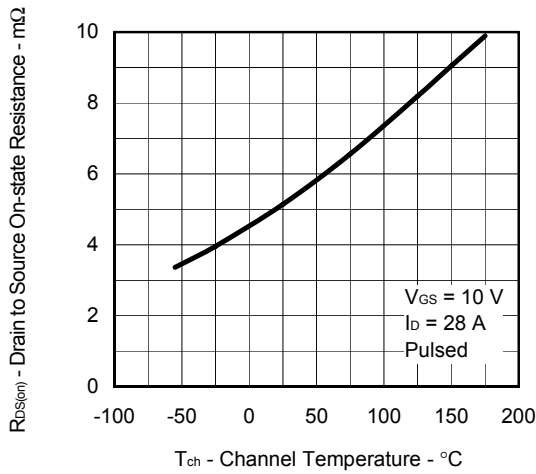
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



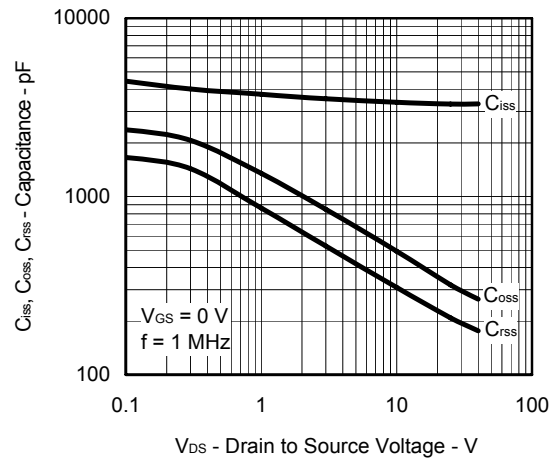
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



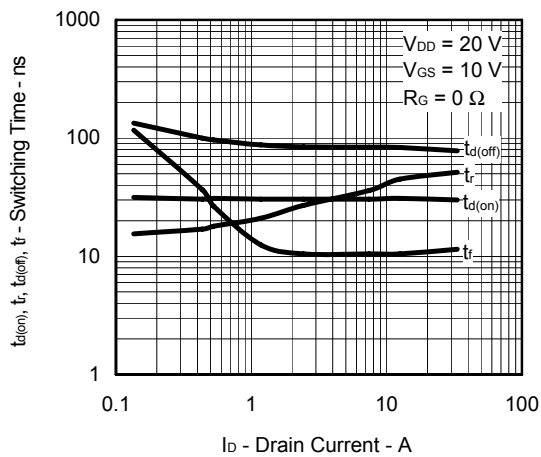
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



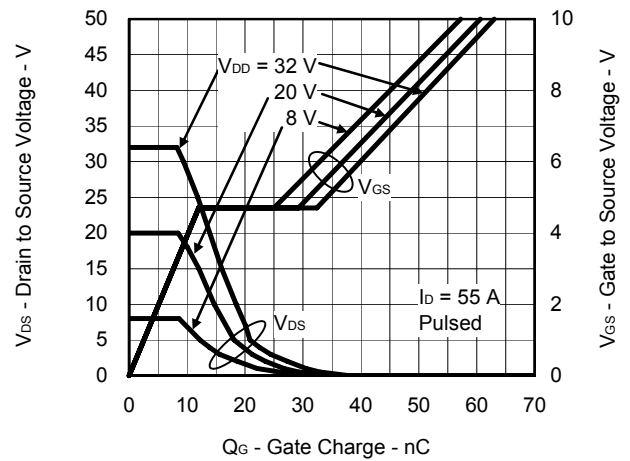
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



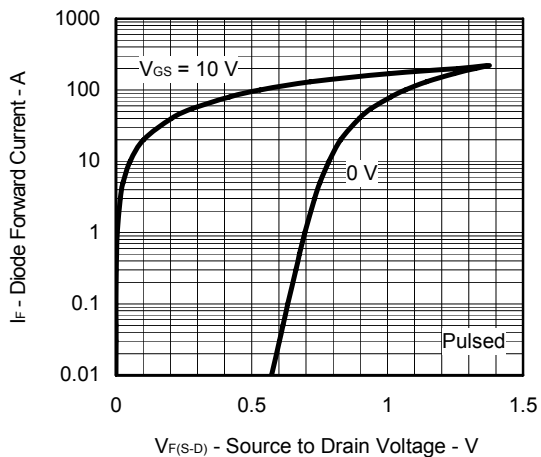
SWITCHING CHARACTERISTICS



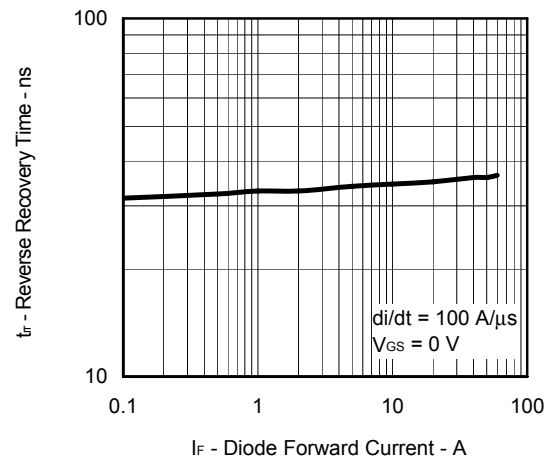
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

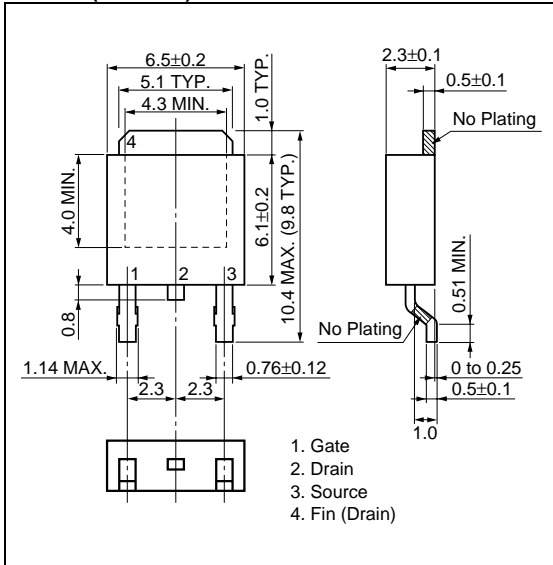


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

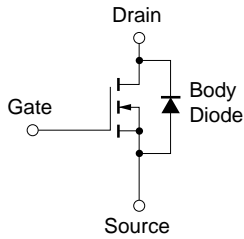


PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.



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